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PATENT APPLICATION

Semiconductor Device Inspection Method

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SEMICONDUCTOR DEVICE INSPECTION METHOD

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a method for inspecting semiconductor devices, liquid crystals, and magnetic heads.

An example in which a semiconductor wafer is inspected will be explained.

2. Description of the Related Art

Semiconductor devices are manufactured by repeating a process that uses lithography or etching to transfer a pattern, usually formed on a photomask, onto a semiconductor wafer. In a semiconductor device manufacturing process, the quality of the lithography or etching, the quality of various other types of processing, and the production of foreign matter can greatly affect the semiconductor device yield. Therefore, methods for inspecting semiconductor wafers from a manufacturing process have conventionally been implemented to detect anomalies or faults early or before they occur.

Methods for inspecting for defects in patterns on semiconductor wafers involve the use of a defect inspection

device that irradiates the semiconductor wafer with white light and uses the optical image to compare the same circuit patterns on a plurality of LSI. For example, as disclosed in Japanese Patent Laid-open H3-167456, in an inspection method that uses optical images, the optically illuminated area on a substrate is imaged on an integrated time delay sensor. Defects are detected by comparing the image detected by the sensor and design information already entered.

In the aforementioned defect inspection, adjoining identical circuit pattern images are formed. These images are then compared and defects automatically detected. However, inspections must also handle wafers that have various pattern layouts or patterns that involve various materials. To accurately compare adjoining patterns, the positioning of the pattern, that is the chip (die) and shot matrice s on the wafer, must be predetermined and preset as inspection conditions for wafers to be inspected. In addition, to enable the formation of images suitable for inspection in various materials, appropriate values must be set for image brightness and the pattern-substrate contrast and these values preset as inspection conditions for wafers to be inspected. However, there are no descriptions of the procedures or operation methods for these inspection condition settings for the above conventional devices and their operation is complex, between one and several hours being required to set appropriate

inspection conditions for a new wafer to be inspected. A problem exists in that, in order to implement pattern inspections for a plurality of products (that is a plurality of circuit pattern matrices) and a plurality of processes (that is a plurality of materials and a plurality of detailed circuit pattern forms) in a semiconductor manufacturing line, a huge number of inspection conditions must be set. As a result, an enormous amount of time is required in all inspection operations and in particular, in inspection condition setting operations.

Japanese Patent Laid-open 2001-35893 discloses a method for improving operation efficiency when the above inspection conditions are set and for reducing the time involved in setting inspection conditions. The design of the operation screen layout reduces the time needed for the entry of setting items but even so, between thirty minutes and several hours are required to set inspection conditions in the inspection device.

Figure 1 is one conventional example of inspection condition settings and shows a conditions setting sequence for a foreign matter inspection device that uses scattered laser light. The conventional setting of inspection conditions starts with preparation of a wafer and loading of that wafer into the device. As preliminary preparation for inspection, the chip matrix within the wafer, the shot matrix when the

pattern is exposed, the chip size, and test element group (TEG) chips for process and yield management must be set so that they will not be inspected and the direction of the wafer scan during the inspection and the chips to be used in alignment must be set. Furthermore, a pattern that uses automatic alignment is selected, the image data of the alignment pattern saved, and actual alignment implemented.

After the above settings are completed, adjustment of the inspection sensitivity starts. Firstly, an spacial filter that efficiently shields diffracted light from repetitive patterns on the chip is set. A trial inspection then takes place. The detection results are confirmed (reviewed) after the trial inspection and a temporary laser power value and threshold value, which are sensitivity conditions, are set. After repeating the sensitivity condition settings, trial inspection and review, and then determining inspection conditions so that less than a certain percentage of false alarms occur, the inspection conditions are saved and the wafer unloaded. This ends the extraction of conditions.

In a device that inspects various types of intricate patterns including those on semiconductor devices as in the above description of conventional technology, various inspection conditions must be set and these conditions must be adjusted for each product and each process. The inspection device is occupied while conditions are being extracted, thus

actually reducing inspection time. Also, because there are a plurality of entry items, a worker who sets conditions requires a certain amount of training and must be experienced in the use of the device. Furthermore, while conditions are being extracted, there is an accumulation of semiconductor products. Therefore, the turnaround time (TAT) of semiconductor devices is extended and costs increase.

SUMMARY OF THE INVENTION

The present invention provides a technology for inspecting intricate circuit patterns that uses images formed by irradiating white light, laser light, or an electron beam, and that minimises user input by using semiconductor device design data when setting the various conditions required for inspection.

By using semiconductor device design data, the present invention also provides a technology that temporarily determines the above inspection condition settings before semiconductor devices requiring inspection reach the inspection process. This minimises the time taken to set inspection conditions.

By using semiconductor device design data, the present invention further provides a technology that produces inspection results, the number of false alarms caused by the

highly sensitive inspection that occur during defect detection being held below a certain percentage thereof.

By using semiconductor device design data, the present invention further provides a technology that judges whether or not detected defects are in areas wherein false alarms are likely to occur, and that, in the setting of inspection conditions, gives priority to the review of defects in areas in which false alarms tend to occur by adding that judgement information to inspection results.

By using semiconductor device design data, the present invention further provides a technology that enables inspection sensitivity to be set to any level to suit the design rules for each area within a semiconductor device chip or to suit the degree of functional importance.

By using semiconductor device design data, the present invention further provides a technology that determines whether defects are in a transparent film or non-transparent film, that adds this information to the detected defect results, and that distinguishes between defects that can and cannot be confirmed using a scanning electron microscope (SEM).

By using semiconductor device design data, the present invention further provides a technology that, in the classification of detected defects, determines if the defect is in a specific pattern or specific material and that obtains information that is useful in defect classification.

In short, according to the present invention, a semiconductor device inspection device is equipped with a function that, through the use of semiconductor device design data, enables a plurality of parameters to be automatically set.

The present invention is also equipped with a function that, through the use of semiconductor device design data, increases the number of detection signal parameters from specific repetitive patterns used in statistical processing during defect detection.

According to the present invention, a semiconductor device inspection device is further equipped with a function that, through the use of semiconductor device design data, adds, to detection results, information as to whether or not the area in which a defect was detected is one in which false alarms tend to occur. The present invention is also equipped with a function that, based on this supplementary information, can isolate and review those defects in areas in which false alarms tend to occur.

The present invention is further equipped with a function that, through use of the semiconductor device design data, determines if the defect is in a transparent film or non-transparent film and that adds this information to the defect detection results.

Also, to achieve the above objects according to the

present invention, the semiconductor device inspection method is configured to set inspection conditions using semiconductor device design data, to inspect semiconductor devices using these set conditions, to then use the results of inspections to revise inspection conditions set using design data, and to inspect semiconductor devices using these revised inspection conditions.

Also, in the present invention, the semiconductor device inspection method is configured to extract related information from a design data base that specifies the product names of semiconductor devices and the names of processes used to process them, that sets inspection conditions using this extracted related information, that inspects semiconductor devices using these set conditions, that then uses the results of inspections to revise set inspection conditions using design data, and that then inspects semiconductor devices using these revised inspection conditions.

These and other objects, features and advantages of the invention will be apparent from the following more particular description of preferred embodiments of the invention, as illustrated in the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a flowchart showing the sequence involved in

setting inspection conditions according to conventional technology;

Figure 2 is a flowchart showing the sequence involved in setting inspection conditions according to the present invention;

Figure 3 is a plan view of a wafer and chip used in the explanation of chip matrix and chip size settings;

Figure 4 is a plan view of a wafer used in the explanation of a shot matrix;

Figure 5(a) is a plan view of a wafer used in the explanation of inspection sequence settings;

Figure 5(b) is a plan view of a chip used in the explanation of inspection sequence settings;

Figure 6 is a plan view of a wafer used in the explanation of settings for chips that will and that will not be inspected;

Figure 7 is a plan view of a chip used in the explanation of settings for chips that will and that will not be inspected;

Figure 8 is a plan view of an alignment pattern;

Figure 9(a) is a plan view of a chip;

Figure 9(b) is a plan view of a chip showing the site of signal acquisition;

Figure 9(c) is a graph showing signal values before spacial filter settings;

Figure 9(d) is a graph showing signal values after spacial filter settings;

Figure 10 is a plan view of a chip;

Figure 11 is an enlarged plan view of a chip showing a defect on the chip;

Figure 12(a) is a plan view of a chip showing the corresponding point on the chip;

Figure 12(b) is a histogram of signal values;

Figure 13(a) is a plan view of a chip showing the corresponding point on the chip;

Figure 13(b) is a histogram of signal values;

Figure 14(a) is a plan view of a chip showing the site of signal acquisition;

Figure 14(b) is a graph showing the relationship between the amount of light and signal values; and

Figure 15 is a plan view of a chip showing an area in which many false alarms occur.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 2 shows an example of a sequence relating to the setting of inspection conditions according to the present invention. Firstly, inspection conditions are temporarily determined prior to the wafer actually arriving at the inspection process. This enables minimisation of wafer

accumulation time while conditions are being set.

Firstly, the product name of the semiconductor device to be inspected and the name of the process in which the semiconductor device is processed immediately prior to inspection are entered from a terminal. When the product name and process name are entered, the semiconductor device design data base is accessed via a communication means and the data required for inspection preliminary preparation collected. The conditions required for inspection are then automatically set in the steps shown in Fig. 2. A worker can enter the product name and process name settings by any means such as a keyboard or a barcode reader. Entries can be made from within a clean room, or from a personal computer outside a clean room that can access the device.

This ends the preliminary preparation for the setting of conditions in an inspection device.

Since there are only two entries to be made, that is, the product name and process name, the worker need not be skilled in the use of the inspection device.

Next, the setting of sensitivity levels after the wafer has actually arrived will be explained.

Alignment automatically starts when the wafer is loaded into the device. After alignment has ended, sensitivity condition settings (laser power, threshold value), a trial inspection, and a review are repeated. Then, after inspection

conditions that enable only actual reviewed and classified defects to be detected and inspection conditions that enable false alarms to be held below a certain percentage are determined, these conditions are saved and the wafer unloaded. This ends the extraction of conditions. These saved inspection conditions and images of reviewed defects can be confirmed on the screen.

After inspection conditions are thus determined, wafers processed in the previous process are sequentially inspected using these determined inspection conditions. Wafers that have been inspected are sent to the next process and processed in that next process. The results of the inspections are displayed on screen and stored in a storage means.

The time involved in work within the conditions setting sequence, other than "sensitivity condition settings", "trial inspection" and "review", will take between several seconds and several tens of seconds.

The time involved in "sensitivity condition settings", "trial inspection" and "review" can be greatly reduced through the use of an automatic defect review (ADR) function and an automatic defect classification (ADC) function. The time required for setting conditions can be greatly reduced to between several minutes and several tens of minutes.

Items that are automatically set after the semiconductor device design data base is accessed in preparation for

inspection device condition settings will be explained below.

Fig. 3 shows settings for a chip matrix and for chip size. There are places on a wafer on which there is no chip pattern and during inspection these chips will not be inspected. For example, touching of the wafer periphery by some parts of chips very close to the periphery of the wafer and film thickness irregularities can cause the semiconductor device to not work. These chips are removed as targets of inspection by automatically deleting them. In a chip size setting, the size in the x-direction of the chip and the size in the y-direction are set.

Fig. 4 shows settings for a shot matrix. When a semiconductor device pattern is exposed, a plurality of chips are sometimes exposed together. In that case, different (same for shot unit) patterns are formed for each chip on the periphery (scribe area) of the chips. Here, when ordinary chips undergo a comparison inspection, a false alarm will sound for the scribe area and the inspection sequence in the scribe area will therefore have to be changed.

Fig. 5(a) shows a shot area on a wafer and Fig. 5(b) shows a diagram of a chip that will be used to explain the inspection sequence and shows how a comparison method is set to suit repetitive units. That is, patterns that are repeated in shot units, such as in the scribe area, are inspected using comparison inspection in shot units. Patterns that are

repeated in chip units are inspected using comparison inspection in chip units, and cell patterns such as in DRAM, SRAM, and FLASH memory are inspected using cell comparison. Because there are minor variations in the size and film thickness of the wafer surface, usually, the smaller the comparison range the lesser the variations, and inspection sensitivity is improved.

Fig. 6 shows an example of settings for chips that will and that will not be inspected. Sometimes a wafer includes test element group (TEG) chips for managing processes and yield. These TEG chips frequently have a circuit pattern that is completely different to that of other chips and so when such chips are inspected, false alarms often occur for the TEG chip. Therefore, TEG chips are usually set so that they will not be inspected.

Fig. 7 shows an example in which areas that will and will not be inspected are set for a chip pattern. In this example, the scribe area is set so that it will not be inspected. This area is cut off when the chip is cut out of the wafer and so it has almost no effect on the operation of a semiconductor device. Therefore, depending on the semiconductor device manufacturer, defects in this area are sometimes excluded from management. Some particular areas, for example the yield of a cache memory area in a CPU product, affect product quality and price, and therefore when settings are being made for areas

that will or will not be inspected, it is possible to set only those areas for inspection.

Fig. 8 shows the settings of an alignment pattern. In alignment, pre-registered patterns and wafer patterns that are targeted for inspection are compared beforehand and these patterns are matched. Therefore, by obtaining form information from design data, the need to capture and save images especially using an actual wafer when setting conditions is eliminated. Also, by using pattern material information, patterns with high contrasts can be set automatically.

Fig. 9(a) shows a chip and an enlarged diagram of a repetitive pattern area on the chip. Fig. 9(b) shows the signal acquisition site on a chip, Fig. 9(c) shows a detection signal acquired from this signal acquisition site prior to spacial filter settings, and Fig. 9(d) shows an example of the spacial filter settings made after a detection signal is acquired from this signal acquisition site. When light shines on a repetitive pattern in a semiconductor product, diffraction of light occurs in accordance with the pitch of the repetitive pattern and the wavelength of the light. By shielding this diffracted light, the spacial filter improves the S/N of the pattern and foreign matter and defects.

Because the wavelength of the lighting is already known in the inspection device, the pattern of diffracted light can

be determined by obtaining the repetitive pattern pitch size from design data. This enables automatic setting of the spacial filter. The bottom section of Fig. 9 shows a comparison before and after the spacial filter settings are made, and thus shows an example of how the pattern signals are lower when the spacial filter is set and how defects that were previously hidden within the pattern signal can now be detected. Spacial filters can also be set for each inspection area. In this case, the noise from patterns in each area can be suppressed to enable highly sensitive detection.

Fig. 10 shows an example in which sensitivity is set for each inspection area. For example, even if there is a 0.1 mm piece of foreign matter in a wiring portion of 0.5 mm pitch, this foreign matter will have almost no effect on yield. That is, too highly sensitive an inspection of this area will result in defects that have no effect on yield, that is defects that do not need to be addressed, being detected, creating a lot of noise for the person at the workplace managing the process. Therefore, by obtaining wiring rules from semiconductor device design data for each area, each area can be inspected with the sensitivity required for that area. Also, the number of the false alarms can be reduced by lowering sensitivity in those areas where false alarms often occur, for example the scribe area.

Fig. 11 is an example that shows the pattern on which a

defect exists by matching the coordinates of the detected defect and the design data. For example, voids have occurred in Cu wiring but there are no voids anywhere other than on that Cu wiring. Therefore, when automatically classifying defects, whether or not a defect exists in a particular amount in Cu wiring is useful information. This information can help to improve the precision of automatic defect classification. In a review using SEM, only defects on the surface can be reviewed because of SEM characteristics. By adding information concerning whether the defects are on the transparent film or the non-transparent film to the defect detection results, an efficient selection of defects that can be targeted by an SEM review is enabled.

Figs. 12 and 13 show examples in inspection devices that perform statistical processing in comparative inspection algorithms, in which stable conditions with few false alarms can be set by increasing the number of the statistical parameters using design data.

Statistical processing in comparative chip inspection postulates a signal value and frequency distribution using either signal from points that correspond to coordinates for each chip or signal differential values. A threshold value is set for the suggested distribution and anything exceeding this value is deemed to be an error. Here, if there are an insufficient number of chips on the wafer, there will be an

insufficient number of parameters when statistics are collected and the reliability of the signal value frequency distribution will decrease. This will mean that false alarms will occur frequently. In this case, a higher threshold value is set and inspection conditions are set such that false alarms will not occur. This will mean that the overall sensitivity drops.

If design data is used, identical signals are obtained for identical patterns even for points other than those that correspond to coordinates for each chip and therefore, the number of parameters can be increased. The reliability of the suggested distribution increases with the increase in the number of parameters and the threshold value can be lowered. As a result, highly sensitive inspection with few false alarms is enabled.

Fig. 14 shows an example of a method in which the amount of light is controlled using the pattern density. The strength of light detected on entry into a sensor varies according to the pattern density and form. There is a dynamic range within the sensor and, for example, if a pattern does not shine very brightly the area cannot be inspected. Design data can be used to estimate, in advance, the amount of light that will be detected in each area. Control of the amount of light during inspection enables inspection of a broad area while maintaining sensitivity. The light control for each

area can be automatically set based on the amount of light detected during the trial inspection.

Fig. 15 shows an area on a chip in which many false alarms occur. During the review that occurs after the trial inspection, areas in which many false alarms occur are isolated and reviewed. This enables the degree to which false alarms are occurring for temporary conditions to be judged in just a short time. This means that the time taken to extract conditions can be reduced.

As explained above, by using semiconductor device design data in the present invention: (1) the number of items that must be entered when setting conditions decreases and thus the time involved in setting conditions can be shortened; (2) the resultant reduction in the number of entry items means that the worker's load is decreased and the amount of training required for use of the inspection device is reduced; and (3) because inspection conditions can be temporarily set without using an actual wafer, the time during which wafers accumulate can be reduced.

The invention may be embodied in other specific forms without departing from the spirit of essential characteristics thereof. The present embodiment is therefore to be considered in all respects as illustrative and not restrictive, the scope of the invention being indicated by the appended claims rather than by the foregoing description and all changes which come

within the meaning and range of equivalency of the claims are therefore intended to be embraced therein.